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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,734	12/28/2001	Salman Akram	2754.4US (95-0742.4)	6382

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EXAMINER
GRAYBILL, DAVID E

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,734	AKRAM ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 6, 18, 20, 24 and 36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 2, 6, 18, 20 and 24 the scope of the limitation, "which is substantially the same as the first semiconductor device," cannot be determined because the property that is the same is not recited or otherwise identified.

In claims 18 and 36 there is insufficient antecedent basis for the language, "the other side."

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15, 17-33, 35 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Corbett (4992849).

At column 4, lines 63-65, column 5, lines 4-40, column 6, lines 34-37 and 59-61, column 6, line 68 to column 7, line 2, column 7, lines 7-10, 22-40 and 54-63, column 8, lines 15-20, 28-29, 40-43 and 52-58, column 8, line 60 to column 9, line 31, column 9, lines 50-53 and column 10, lines 10-13 and 27-28, Corbett teaches the following:

1. A multi-chip module system comprising: a substrate 23 having at least a first position ["die receiving portions"] having, in turn, a predetermined configuration for locating a first semiconductor device thereat and having at least one other vacant position ["second set of circuit traces"] having, in turn, a predetermined configuration for locating a second semiconductor device thereat on the multi-chip module system; and a first semiconductor device [one of 31] located in the at least first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic.

2. The multi-chip module system of 1, further comprising: the at least one other vacant position having the predetermined configuration for locating the second semiconductor device

thereat which is substantially the same as the first semiconductor device.

3. The multi-chip module system of 1, further comprising: the at least one other vacant position having the predetermined configuration for locating the second semiconductor device thereat; and the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

4. The multi-chip module system of 1, further comprising: the at least one other vacant position having the predetermined configuration for locating the second semiconductor device thereat; and the second semiconductor device having a second predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

5. A multi-chip module system comprising: a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position ["die receiving portions"] having, in turn, a predetermined configuration for locating a second semiconductor device thereat, and having at least one other vacant position having, in turn, a predetermined configuration for locating a

third semiconductor device thereat on the multi-chip module system; the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and the second semiconductor device [another of 31] located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic.

6. The multi-chip module system of 4 further comprising: the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat which is substantially the same as the first semiconductor device.

7. The multi-chip module system of 4 further comprising: the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and the third semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

8. The multi-chip module system of 4 further comprising: the at least one other vacant position having a predetermined

configuration for locating a third semiconductor device thereat; and the third semiconductor device having a predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

9. The multi-chip module system of 4, further comprising: the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and the third semiconductor device having a predetermined performance characteristic of at least substantially three times greater than that of the second predetermined performance characteristic of the second semiconductor device.

10. The multi-chip module system of 4 further comprising: the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and the third semiconductor device having a predetermined performance characteristic of at least substantially four times greater than that of the first and the second predetermined performance characteristic of the first semiconductor device and the second semiconductor device combined.

11. The multi-chip module system of 4, wherein the first semiconductor device comprises a memory device.

12. The multi-chip module system of 4, wherein the second semiconductor device comprises a memory device.

13. The multi-chip module system of 4, wherein the first semiconductor device comprises a microprocessor device.

14. The multi-chip module system of 4, wherein the second semiconductor device comprises a microprocessor device.

15. The multi-chip module system of 4, wherein the multi-chip module system comprises a single in-line memory module system.

17. A multi-chip module system comprising: a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, having a first vacant position ["second set of circuit traces"] having, in turn, a predetermined configuration for locating a third semiconductor device thereat, and having a second vacant position ["second set of circuit traces"] having, in turn, a predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system; the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and the second semiconductor device located in

the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic.

18. The multi-chip system module of 17, wherein: the first vacant position located on the substrate is located on one side of the substrate; and the second vacant position located on the substrate is located on the other side of the substrate.

19. A multi-chip module system comprising: a substrate having at least a first predetermined configuration position for locating a first semiconductor device thereat and having at least one other vacant predetermined configuration position for locating a second semiconductor device thereat on the multi-chip module system; and the first semiconductor device located in the at least the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic.

20. The multi-chip module system of 19, further comprising: the at least one other vacant predetermined configuration position for locating the second semiconductor device thereat which is substantially the same as the first semiconductor device.

21. The multi-chip module system of 19, further comprising: the at least one other vacant predetermined configuration position

having a predetermined configuration for locating the second semiconductor device thereat; and the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

22. The multi-chip module system of 19, further comprising: the at least one other vacant predetermined configuration position having a predetermined configuration for locating the second semiconductor device thereat; and the second semiconductor device having a predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

23. A multi-chip module system comprising: a substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, and having at least one other vacant predetermined configuration position for locating a third semiconductor device thereat on the multi-chip module system; the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device

having a first predetermined performance characteristic; and the second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic.

24. The multi-chip module system of 23, further comprising: the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat which is substantially the same as the first semiconductor device.

25. The multi-chip module system of 23, further comprising: the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat; and the third semiconductor device having a third predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

26. The multi-chip module system of 23, further comprising: the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat; and the third semiconductor device having a third predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

27. The multi-chip module system of 23, further comprising: the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat; and the third semiconductor device having a third predetermined performance characteristic of at least substantially three times greater than that of the second predetermined performance characteristic of the second semiconductor device.

28. The multi-chip module system of 23, further comprising: the at least one other vacant predetermined configuration position for locating a third semiconductor device thereat; and the third semiconductor device having a third predetermined performance characteristic of at least substantially four times greater, than that of the first and second predetermined performance characteristic of the first semiconductor device and the second semiconductor device combined.

29. The multi-chip module system of 23, wherein the first semiconductor device comprises a memory device.

30. The multi-chip module system of 23, wherein the second semiconductor device comprises a memory device.

31. The multi-chip module system of 23, wherein the first semiconductor device comprises a microprocessor device.

32. The multi-chip module system of 23, wherein the second semiconductor device comprises a microprocessor device.

33. The multi-chip module system of 23, wherein the multi-chip module system comprises a single in-line memory module system.

35. A multi-chip module system comprising: a substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, having a first vacant predetermined configuration position for locating a third semiconductor device thereat, and having a second vacant predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system; the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and the second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic.

36. The multi-chip module of 35, wherein: the first vacant predetermined configuration position located on the substrate is located on one side of the substrate; and the second vacant predetermined configuration position located on the substrate is located on the other side the substrate.

To further clarify the teaching of vacant positions having predetermined configurations for locating semiconductor devices, it is noted that the scope of claim 1 encompasses vacant "second set of circuit traces" portions. Furthermore, claim 7 confirms that the vacant positions are for locating integrated circuit semiconductor devices.

Also, the claims are replete with statements of intended use that do not result in a structural difference between the claimed product and the product of Corbett. Most of these statements of intended use are preceded by the preposition "for." The following is a non-exhaustive list of examples of these statements of intended use: for locating a first semiconductor device thereat; for locating a second semiconductor device thereat; for locating the second semiconductor device thereat which is substantially the same as the first semiconductor device; for locating a third semiconductor device thereat which is substantially the same as the first semiconductor device. Because the product of Corbett is inherently capable of being used for the intended uses the statements of intended use do not patentably distinguish the claimed product from the product of Corbett. Claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531

(CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

To further afford applicant the benefit of compact prosecution, it is noted that the scope of the claims which include elements introduced solely by statements of intended use is not limited to the presence of those elements. For example, the scope of claims 1-4 and 6-15 encompasses a product not comprising a second or third semiconductor device.

To further clarify the teaching that the first vacant position located on the substrate is located on one side of the substrate, and the second vacant position located on the substrate is located on the other side of the substrate, it is noted that, as cited, Corbett teaches, "a second set of circuit traces on a plane which is separate from said one side of the polymeric sheet."

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 16 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corbett as applied to claims 1-15, 17-33, 35 and 36, and further in combination with Derouiche (5623395).

Corbett does not appear to explicitly teach the following: 16. The multi-chip module system of 4, further comprising: a third semiconductor device; and an adapter connected to the third semiconductor device, the adapter having a configuration for connecting the adapter to the at least one other vacant position on the substrate to connect the third semiconductor device to the substrate.

34. The multi-chip module system of 23, further comprising: an adapter connected to the third semiconductor device, the adapter for connecting the adapter to the at least one other vacant predetermined configuration position an the substrate to connect the third semiconductor device to the substrate.

Nonetheless, at column 4, lines 16-36, Derouiche teaches an adapter 42 connected to a semiconductor device 30a, the adapter for connecting the adapter to a vacant predetermined configuration position on a substrate to connect the semiconductor device to the substrate.

Moreover, it would have been obvious to combine the product of Derouiche with the product of Corbett because it would facilitate connection of a semiconductor device to the substrate of Corbett.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.

David E. Graybill
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Art Unit 2827

D.G.
1-Aug-02